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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,903	10/28/2003	Koji Muranishi	031948-3	3959

22204 7590 11/27/2006

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EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,903	MURANISHI, KOJI	
	Examiner	Art Unit	
	Ryan C. Jager	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-5 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Pan (USP 6348823).

With respect to claim 1, figure 7A of Pan discloses a phase adjustment circuit receives a first pair of clock signals (704, 708) and outputs a second pair of clock signals (710,708) with phases satisfying a predetermined condition to a central processing unit, comprising:

a clock proliferator (734) receives a first clock signal (704) and generates a plurality of clock signals therefrom (outputs from 734 to 732);

a clock selector (732) receives said plurality of clock signals from the clock proliferator, selects one of the received plurality of clock signals in accordance with a selection signal (726), and outputs the selected clock signal (710); and

a phase difference detector (612) that receives the selected clock signal (710) and a second clock signal (708) differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal (714) indicating whether the predetermined condition is satisfied;

the first clock signal (704) and the second clock signal (708) constituting the first pair of clock signals;

the second clock signal (708) and the selected clock signal (710) constituting the second pair of clock signals.

Note that the limitation of providing the output clocks to a CPU is recited in the preamble and is considered a statement of intended use. The circuit disclosed in figure 7A of Pan is fully capable of providing clocks to a CPU and the limitation is met.

With respect to claim 2, figure 7A of Pan discloses the phase adjustment circuit of claim 1, wherein the clock proliferators generates the plurality of clock signals by delaying the first clock signal by different amounts (shown if fig. 8A element 734).

With respect to claim 3, figure 7A of Pan discloses the phase adjustment circuit of claim 2, wherein the clock proliferators comprises a cascaded plurality of delay elements (see figure 8A element 734).

With respect to claim 4, figure 7A of Pan discloses the phase adjustment circuit of claim 1, further comprising:

an external input terminal for input of the selection signal (726); and

an external output terminal for output of the detection signal (714).

With respect to claim 5, figure 7A of Pan discloses the phase adjustment circuit of claim 1, further comprising:

an externally writable register (728) that stores the selection signal (726) and providing the selection signal to the clock selector; and

an external output terminal for output of the detection signal (726).

With respect to claim 10, figure 7A of Pan discloses the phase adjustment circuit of claim 1, further comprising a selection signal generator (730 and 606) that receives the detection signal (714) and generates the selection signal (SUM).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (USP 6348823) in view of Kuwata (USP 6959061).

With respect to claims 6 and 8, figure 7A of Pan discloses a phase adjustment circuit for receiving a first pair of clock signals (704 and 708) and outputting a second pair of clock signals (708 and S0) with phases satisfying a predetermined condition, comprising: a clock proliferator (734) for receiving a first clock signal (704) and generating a plurality of clock signals therefrom; a clock selector (732) for receiving said plurality of clock signals from the clock proliferator, selecting one of the received plurality of clock signals in accordance with a selection signal (726), and outputting the selected clock signal (S0); and a phase difference detector (612) for receiving the selected clock signal (S0) and a second clock signal (708), determining whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputting a detection signal (714) indicating whether the predetermined condition is satisfied; the first clock signal (704) and the second clock signal (708) constituting the first pair of clock signals; the second clock signal (708) and the selected

clock signal (S0) constituting the second pair of clock signals. Figure 7A of Pan does not disclose a phase adjustment circuit comprising: a first flip-flop for latching and outputting the state of the second clock signal at rising edges of the selected clock signal; a second flip-flop for latching and outputting the state of the second clock signal at falling edges of the selected clock signal; and a logic circuit for performing a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal. However, figure 5 of Kuwata discloses a phase detection circuit comprising a first flip-flop (13a) for latching and outputting the state of the second clock signal (data) at rising edges of the selected clock signal (clk); a second flip-flop (13b) for latching and outputting the state of the second clock signal (data) at falling edges of the selected clock signal (clk); and a logic circuit (inverter 13d' and NAND 13e) for performing a logic operation on outputs of the first flip-flop (13a) and the second flip-flop (13b), thereby generating the detection signal (ESPD) that is held at a fixed value to prevent erroneous synchronization. Therefore it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit of in figure 1 of Takeshi by replacing the phase detector (7, figure 1) with the phase detector (13, figure 5) of Kuwata for the purpose of eliminating the possibility of erroneous synchronization (col9, lines 39-51).

With respect to claim 9, the above modification discloses the phase adjustment circuit of claim 8, wherein the first clock signal (704) has a higher frequency than the second clock signal (708).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (USP 6348823) in view of Kuwata (USP 6959061).

With respect to claim 7, the modification in the rejection of claims 6, 8 and 9 discloses all the limitations of this claim except that the frequency of the second clock is higher than the frequency of the first clock. However, it would have been obvious to one skilled in the art at the time the invention was made to modify the above modification by programming the programmable divider (738) of Pan to produce a frequency that is higher than the first clock (704) signal frequency for the second clock (708) for the purpose of producing a desired higher frequency in the selected output clock signal.

Response to Arguments

4. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant's arguments filed 10/05/2006 have been fully considered but they are not persuasive.

With respect to applicants argument the Pan does not disclose or suggest a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied. However, this argument is not persuasive because Figure 7B of Pan discloses the different frequencies between the second (708) clock and the first (704) and selected clock (710 or S0) and a phase detection circuit (612) that outputs a detection signal (714).

Allowable Subject Matter

6. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Jager whose telephone number is (571) 272-7016. The examiner can normally be reached on M-F 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RCJ

Ryan C. Jager
11/15/2006

LONG NGUYEN
PRIMARY EXAMINER